Aitken Configuration Details

Aitken (pronounced AY-ken) is a modular computing system housed in NASA's Modular Supercomputing Facility, located less than a mile from the main NAS building. Aitken is configured as follows:

Intel Cascade Lake-Based Compute Resources

- 4 E-Cells (8 E-racks)
- 1,152 Cascade Lake nodes
- 46,080 cores
- 221 terabytes (TB) total memory
- 3.69 petaflops (PF) theoretical peak performance

AMD Rome-Based Compute Resources

- 12 racks
- 1,536 Rome nodes
- 196,608 cores
- 786 TB total memory
- 7.08 PF theoretical peak performance

Hostnames

For the Cascade Lake-based resources, there are four enclosures (individual rack units, or IRUs) in each E-rack, with 36 compute nodes per enclosure. For every two racks, there is a rack leader controlling them. The naming convention for the 288 nodes residing in every two racks (2 racks x 4 enclosures x 36 nodes) uses only odd rack numbers. Therefore, the hostnames of the Aitken compute nodes are r[x]i[0-7]n[0-35], where x are odd numbers between 901 and 907.

For the Rome-based resources, there are four enclosures in each rack, eight compute trays in each enclosure, and four nodes in each compute tray. The hostnames of the Aitken Rome nodes are r[x]c[1-4]t[1-8]n[1-4], where x are numbers between 201 - 208 and 213 - 216.

Processor, Memory, and Network Subsystems Statistics

The following table provides detailed configuration statistics for the processor, memory, and network subsystems for the Aitken compute nodes:

Aitken Processor, Memory, and Network Subsystems Statistics

Architecture	HPE SGI 8600-XA730i Gen10	HPE Apollo 9000
	Processor	
	Cascade Lake	**Rome**
CPU	20-Core Xeon Gold 6248	64-Core EPYC 7742
Newest Instruction Set	AVX-512	AVX2
Hyper-Threading	ON	OFF
TurboBoost	ON	ON

non-Turbo base CPU-Clock	2.5 GHz	2.25 GHz
Maximum Double Precision Floating Point Operations per Cycle per Core	32	16
# of Cores/node	40	128
Total # of Nodes	1,152	1,536
Total # of Cores	46,080	196,608
Total Double Precision TFlops	3,686	7,080
	Memory	
L1 Cache	Local to each core; Instruction cache: 32K Data cache: 32K; Associativity: 8; Cache line size: 64B	Local to each core; Instruction cache: 32K Data cache: 32K; Associativity: 8; Cache line size: 64B
L2 Cache	1 MB per core; Associativity: 16; Cache line size: 64B	512 KB per core; Associativity: 8; Cache line size: 64B
L3 Cache	27.5 MB shared non-inclusive by the 20 cores; Associativity: full; Cache line size: 64B	16 MB shared among 4 cores in a core complex; 256 MB per socket; Associativity: 16; Cache line size: 64B
TLB	Local to each core	Local to each core
Default Page Size	4 KB	4 KB
Memory/Core	4.8 GB; DDR4	4.0 GB; DDR4
Total Memory/node	192 GB	512 GB
Memory Speed and Bandwidth	2,933 MHz; 6 channels; 141 GB/sec read/write	3,200 MHz; 8 channels; 204.8 GB/sec read/write
Inter-socket Interconnect	Ultra-Path Interconnect; 5.2 GHz, 10.4 GT/s, or 62.4 GB/sec	Global Memory Interconnect; 8.0 GHz, 16.0 GT/s, or 96.0 GB/sec
	Inter-node Network	
IB Device on Node	Dual single-port 4x EDR IB Mezzanine card (2 single-port HCAs); 100 Gbits/s	Dual single-port 4x HDR IB Mezzanine card (2 single-port HCAs); 200 Gbits/s
IB Switches Between Nodes	4x HDR; 200 Gbits/s	4x HDR; 200 Gbits/s

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https://www.nas.nasa.gov/hecc/support/kb/entry/580/